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Engineering Note

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Project: Central Fiber Tracker
Doc. No: A1002801

Subject: Bus structures in the 12-MCM AFE as opposed to the 8-MCM AFE

Introduction

In an effort to minimize the number of PC board revisions in the CFT system, the 12-MCM AFE is being touted as having sufficient capability to handle CPS Axial, CPS Stereo, CFT Stereo and FPS fibers all in one layout. This is accomplished through a motherboard-daughterboard structure which places 8 MCMs as dual-range discriminators on the daughter card and four MCMs as single-range units on the motherboard. The different subsystems require that the data be passed around differently on the same layout.

This is accomplished through the use of reconfigurable CPLDs and crosspoint switch logic components. This document shows the bus structures that are implemented for each of the three subsystems that use the 12-MCM AFE, using the same layout for all three boards. Only the basic bus structure is shown here. Details of the PLD and crosspoint implementation will follow. It is presumed that the crosspoint will be implemented using either standard PLDs or, perhaps, specialized PLDs such as the Lattice ispGDX series.

CPS Stereo and CFT Stereo

The simplest variation simply collects up all the fibers and blasts them out, as shown in Figure 1. 128 CFT Stereo fibers are landed onto the motherboard and pass through the motherboard links to the outside world. 128 CPS Stereo fibers go to the daughter card, get digitized into 256 bits and send out three LVDS links from the daughter. Couldn't be easier. Crosspoint resources on both mother and daughter are simple pass-through devices.

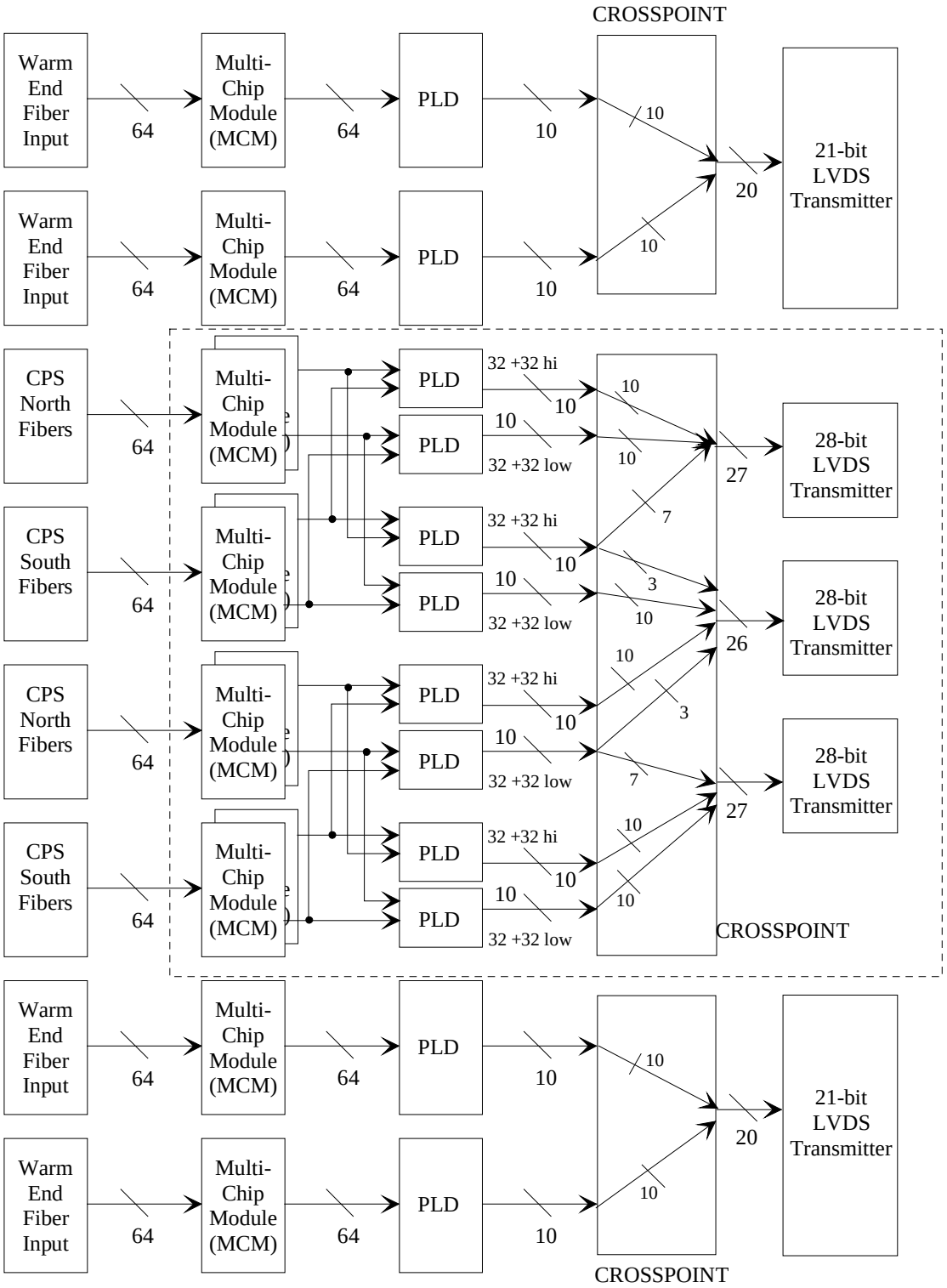

Figure 1 - CPS Stereo/CFT Stereo

CPS Axial/CFT Stereo

In the second pass, the CFT Stereo fibers are handled the same way, but the CPS fibers are not. CPS Axial fibers are ORed in pairs so as to electronically reconnect the North and South halves. This halves the number of bits required to fall out of the daughter card, and so allows the middle link to go unused. It need not be stuffed. The PLDs are reprogrammed to perform the OR, and the crosspoint on the daughter does the rest.

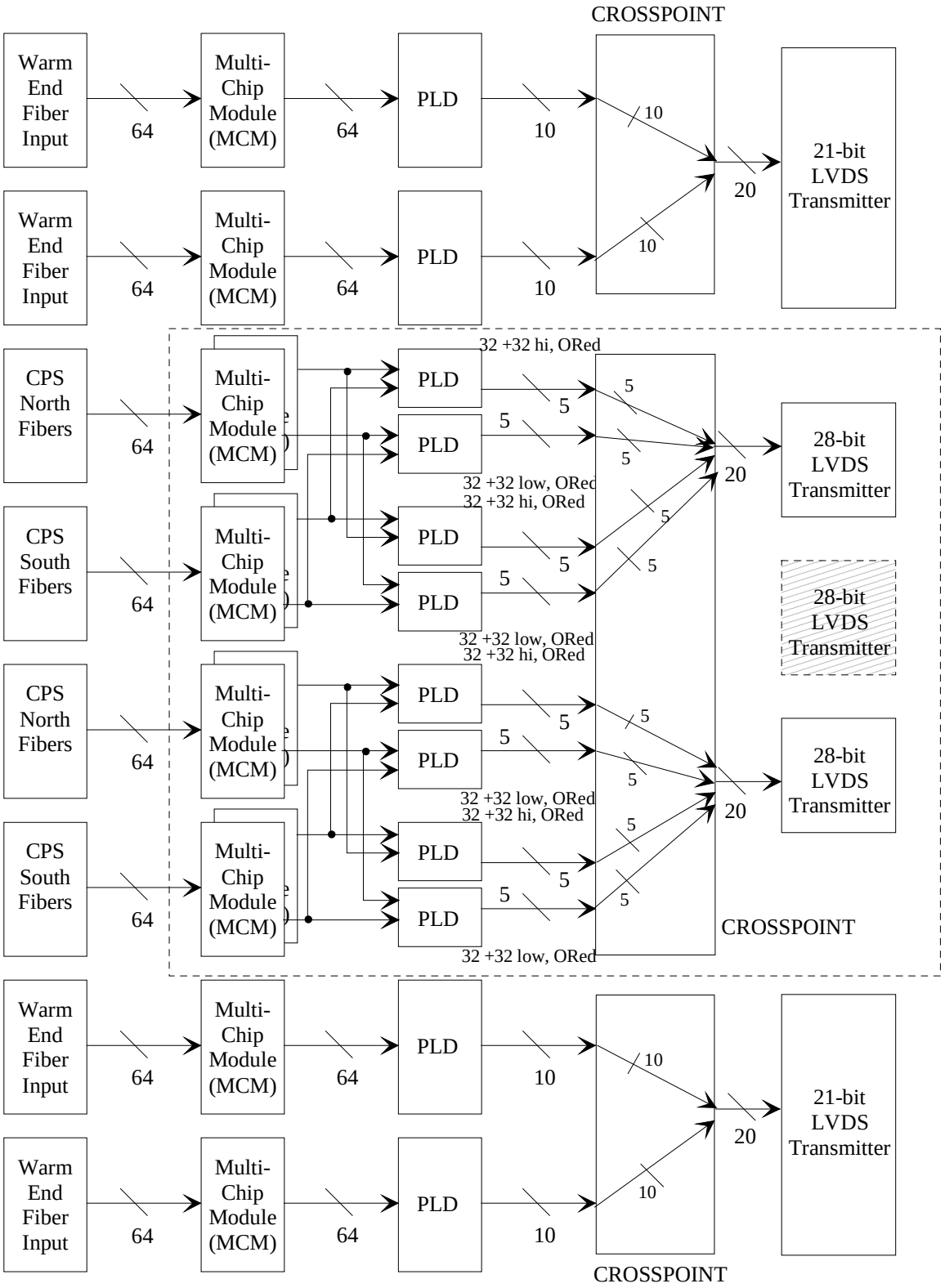

Figure 2 - CPS Axial/CFT Stereo

FPS

Yep, this is the ugly duckling of the group. By-72 organization of the FPS wedges means that we have to share some fibers between connectors on the inputs to get four wedges worth into the daughter card. And, once all 288 fibers on the daughter card have been digitized to create 576 bits of data, there's no way to fit that into three LVDS links, so a few bits spill over onto the motherboard links. The PLDs of the daughter get reprogrammed again, the crosspoint on the daughtercard gets a third layout, and now the crosspoints on the motherboard are required to collect data for the motherboard links.

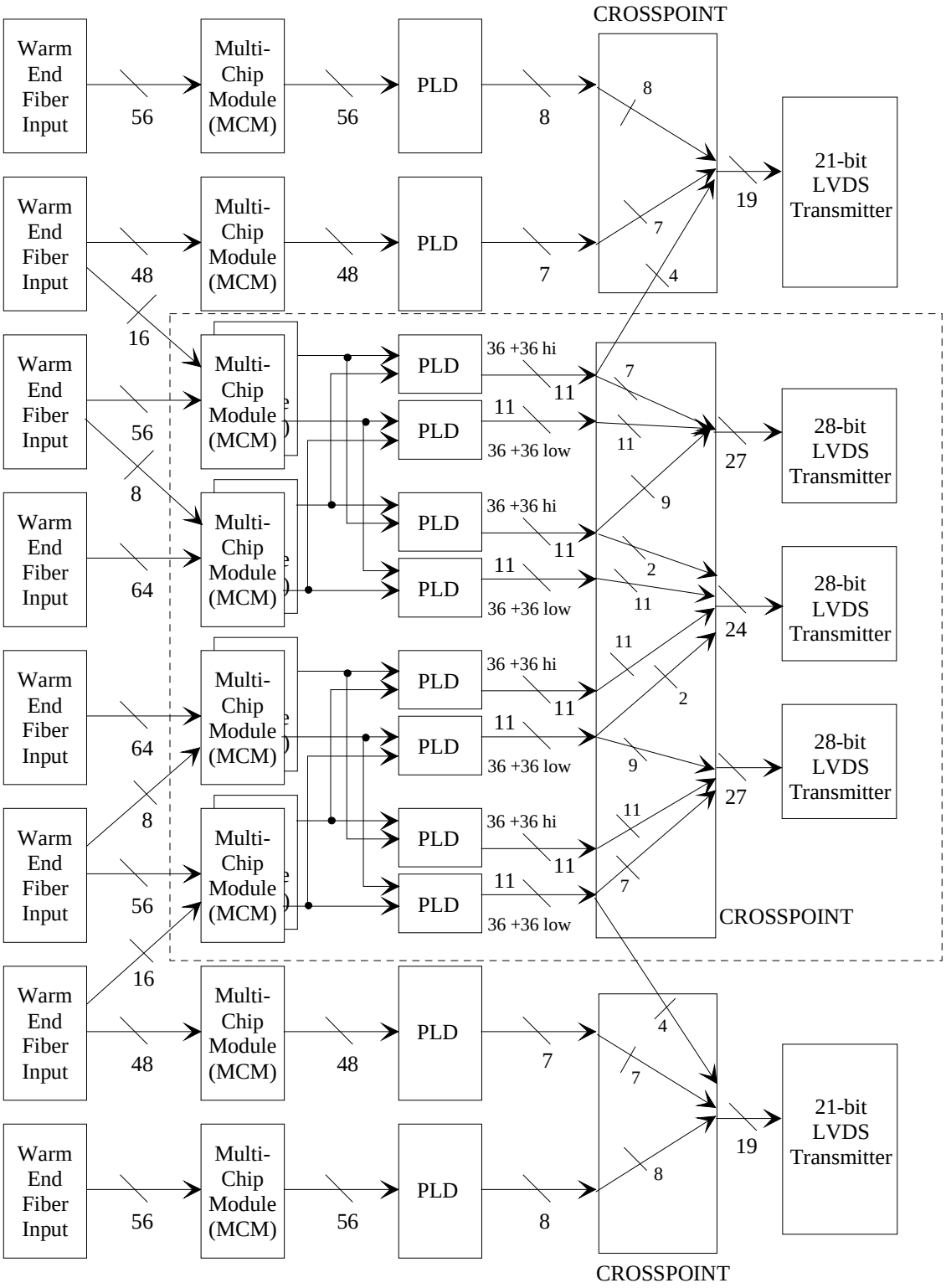

Figure 3 - FPS bus structure